Customer No.: 31561
Application No.: 10/709,954
Docket No.: 11530-US-PA

In The Specification:

Please amend the title to "ELECTRICAL PACKAGE CAPABLE OF INCREASING THE DENSITY OF BONDING PADS AND FINE CIRCUIT LINES INSIDE A INTERCONNECTION".

Please amend paragraphs [0011], [0012], [0013], [0022], [0023], [0035] and [0037] as follows:

[0011] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides an electrical package. The electrical package at least comprises a multi-layer interconnection structure, at least an electronic device and a support substrate. The multi-layer interconnection structure has a top surface and a bottom surface. Furthermore, the multi-layer interconnection structure has an inner circuit with a plurality of bonding pads. The bonding pads are located on the bottom surface of the multi-layer interconnection structure. In addition, the electronic device is disposed on the top surface of the multi-layer interconnection structure but electrically connected to the inner circuit within the multi-layer interconnection structure. The support substrate is fabricated using a conductive material. Furthermore, the support substrate is disposed on the bottom surface of the multi-layer interconnection structure. The support substrate also has a plurality of openings ~~that exposes~~, and each opening exposes one of corresponding bonding pads.

[0012] This invention also provides a method of forming an electrical package. First, a support substrate fabricated using a conductive material is provided. Thereafter, a multi-layer interconnection structure is formed on the support substrate. The multi-layer interconnection structure encloses an inner circuit with a plurality of bonding pads located at the junction interface between the multi-layer interconnection structure and the support substrate. A plurality

of openings that exposes various bonding pads ~~is~~ are formed over the support substrate. At least an electronic device is disposed on the surface of the multi-layer interconnection layer far away from the support substrate. The electronic device is electrically connected to the inner circuit within the multi-layer interconnection structure.

[0013] This invention uses a support substrate with high stiffness, high electrical conductivity, high thermal conductivity and low coefficient of thermal expansion (CTE) to serve as a base layer for building a multi-layer interconnection structure. Thereafter, a plurality of openings that exposes a multiple of bonding pads on the bottom surface of the multi-layer interconnection structure ~~is~~ are formed ~~over~~ in the support substrate. An electronic device is formed over the multi-layer interconnection layer and contacts are formed inside the openings above the bonding pads. Consequently, this invention effectively improves the electrical performance and the heat-dissipating capacity and reduces overall thickness of the electrical package so that the package can be further miniaturized

[0022] As shown in Fig. 2B, ~~a plurality of barrier layers~~ a patterned barrier layer 204 ~~are~~ is formed over the support substrate 202. The barrier ~~layers~~ layer 204 ~~are~~ is fabricated using a metallic material such as gold.

[0023] As shown in Fig. 2C, a multi-layer interconnection structure 206 is formed over the support substrate 202 to cover the barrier ~~layers~~ layer 204. The multi-layer interconnection structure 206 comprises a plurality of circuit layers 208, at least a dielectric layer 210 and a plurality of conductive vias 212. The circuit layers 208 are sequentially stacked over the support

substrate 202. Each dielectric layer 210 is positioned between two neighboring circuit layers 208. The conductive vias 212 pass through one of the dielectric layers 210 to connect at least two circuit layers 208. The circuit layers 208 and the conductive vias 212 together form a network of inner circuits. The inner circuits ~~forms~~ form a plurality of bonding pads 208a located on the top surface 206a of the multi-layer interconnection structure 206. Furthermore, ~~The~~ the inner circuits forms a plurality of bonding pads 208b located on the bottom surface 206b of the multi-layer interconnection structure 206. The bonding pads 208a may be respectively formed with a portion of the circuit layers 208 or a portion of the conductive vias 212. In Fig. 2C, the bonding pads 208a are respectively formed with a portion of the conductive vias 212. In addition, the circuit layers 208 are fabricated from a metallic material such as copper, aluminum or an alloy of the two. The dielectric layer 210 is fabricated using a dielectric material such as silicon nitride, silicon oxide or epoxy resin.

[0035] As shown in Fig. 4C, a ~~plurality of barrier layers~~ patterned barrier layer 304a and a plurality of conductive vias 304b are formed over the support substrate 302. The barrier ~~layers~~ layer 304a is set up over the isolating layer 322 and the conductive vias 304b are set up inside various openings 322a. The barrier ~~layers~~ layer 304a and the conductive vias 304b are fabricated using a conductive material such as gold.

[0037] As shown in Fig. 4E, a portion of the support substrate 302 is removed to form a plurality of openings 303. Thereafter, a plurality of openings 323 is formed in the isolating layer 322 by ultrasonic drilling, laser burning or plasma etching. The openings 323 are linked to the

various openings 303 so that the bonding pads 308a are indirectly exposed through the barrier ~~layers~~ layer 304a and the conductive vias 304b. Similarly, a pre-solder bump 314 (or a bump) may also be formed over the bonding pad 308a to facilitate flip chip bonding before the electronic device 318 is attached to the top surface 306a of the multi-layer interconnection structure 306. Note that the conductive support substrate 302 instead of a conventional plated line can be used to form various pre-solder bumps 314 on the bonding pads 308a of the multi-layer interconnection structure 306 by plating.